Tutorial 4 - SS2016
Communication Systems and Protocols

Institute for Information Processing Technologies - ITIV
Dr.-Ing. Jens Becker • Dipl.-Inform. Tanja Harbaum

Task 1: I²C-Bus Synchronization

Three I²C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is neglectably small (0 time steps). The individual masters want to establish a clock signal according to the following table 1.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 1.1: clock signals

Assume that Master B is initiating the communication cycle.

A) In general, which functionality does the I²C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node?

B) Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal.

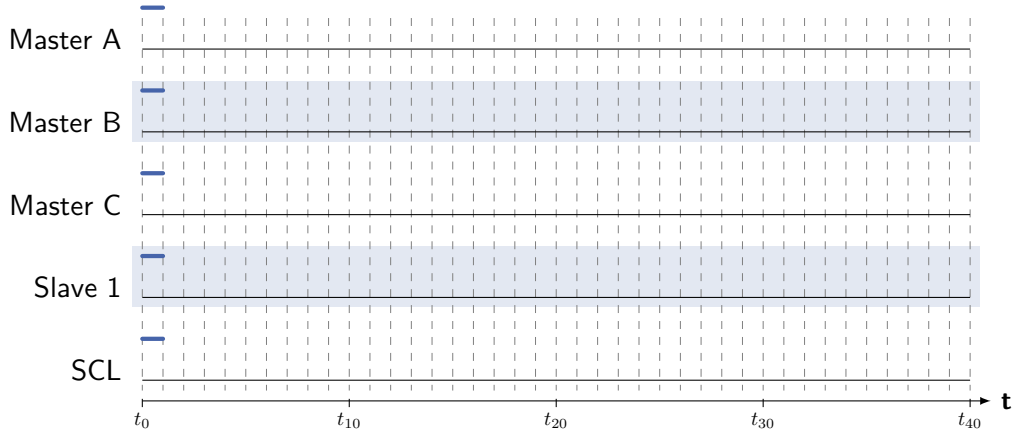

Figure 1.1: Signal sequence

C) In general, which functionality does the I2C bus provide for the case of a master node needing to communicate with a slower slave node?

Task 2: Cyclic Redundancy Check

Task 2.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial.

B) What is the length of the checksum that is to be appended to the data stream?

C) c) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101.

Task 2.2: Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A) Denote the bit stream as it arrives at the receiving node.

B) Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used.
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

Task 2.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$).

Task 3: Actuator Sensor Interface (ASI)

In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 3.1.

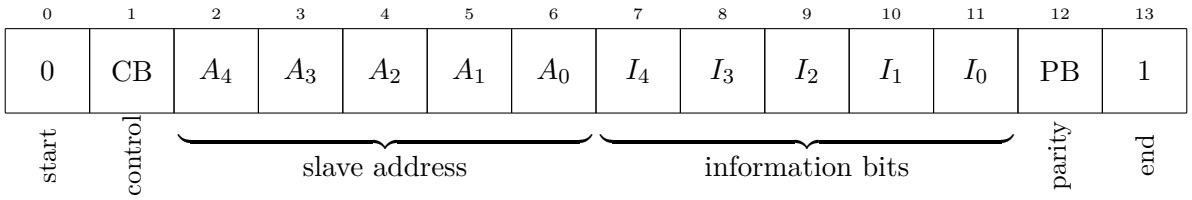

Figure 3.1: ASI packet format, master call

A) Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 3.2 and Manchester as per IEEE 802.3

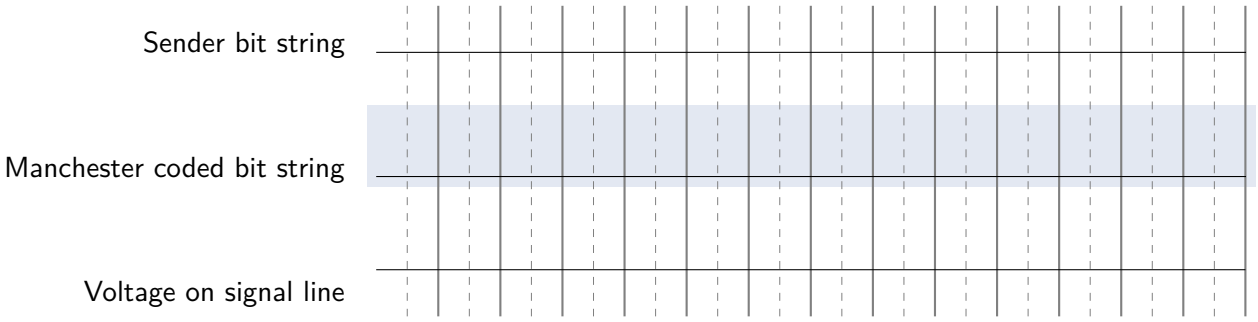

Figure 3.2: Waveform of the sender voltage

B) Figure 3.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

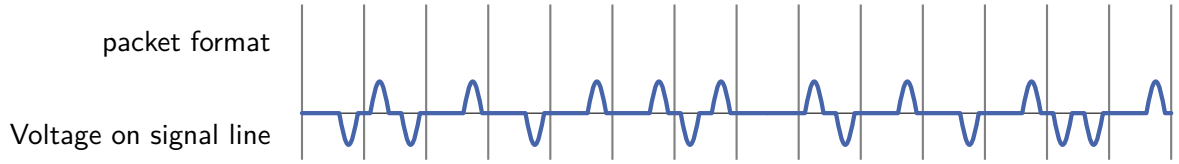

Figure 3.3: Waveform of the sender voltage

Task 4: I²C-Bus Arbitration

The frame format of I²C-bus is shown in figure 4.1. Three master nodes are simultaneously trying to transmit one byte of data to different slaves over the I²C-bus.

S	slave address	$R/\bar{W}$	A	DATA	A	DATA	$A/\bar{A}$	P

data transfered (n bytes + acknowledge)

term	descripion
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave
$\bar{A}$	not acknowledge
DATA	8-bit data
P	stop Condition

Figure 4.1: I²C-bus frame format

A) The addresses of the slaves and the data to be send to them is shown in the table 4.1. Complete the signal diagram in the figure 4.2.
Hint: A slave always answers with a positive Acknowledge (0).

node	slave address	data
Master 1	0100110	00011010
Master 2	0100101	10100111
Master 3	0100101	00101101

Table 4.1: test

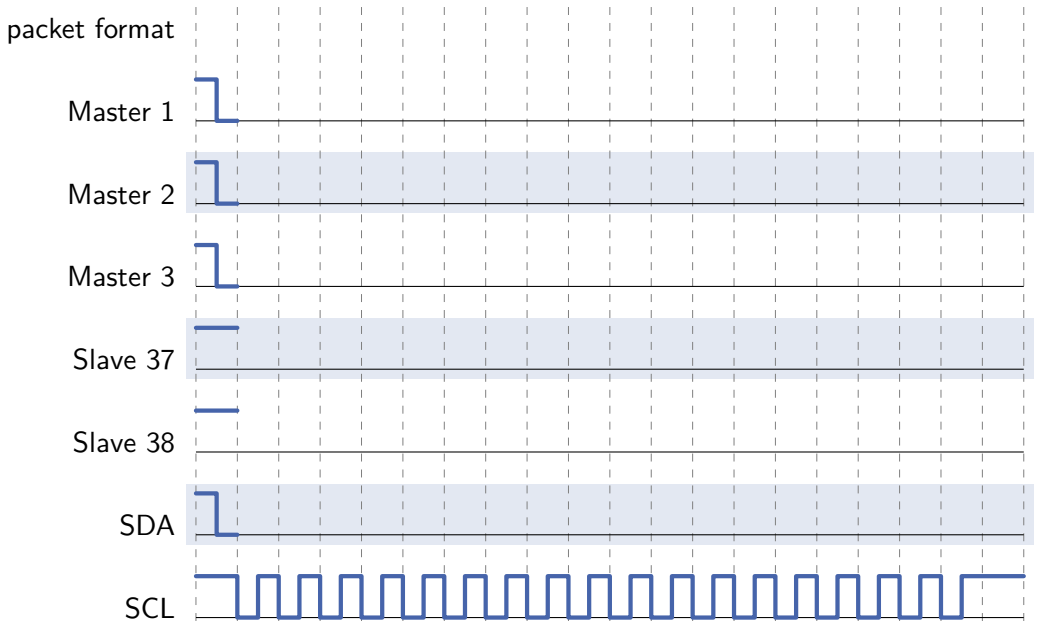

Figure 4.2: Signal sequence

B) Which node is winning the arbitration?

C) Can an I^2C master node change the priority of a slave node during runtime of the system?